

INDIAN MARITIME UNIVERSITY
(A CENTRAL UNIVERSITY, GOVT. OF INDIA)
End Semester Examination December 2018
B. Tech. (Marine Engineering)
Semester - III
Electronics (UG11T2302)

Date: 29-12-2018
Time: 3 Hrs.

Max Marks: 100
Pass Marks: 50

PART – A

Marks:10X3=30

(All questions are compulsory)

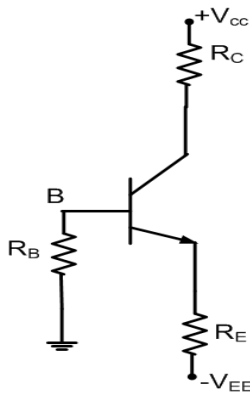
1. (a) Make a T-flip-flop using J-K flip-flop and show its truth table?
(b) What is *input offset* voltage related to OPAMP ?
(c) What is Stack Pointer in microprocessor 8085?
(d) Add two BCD number 1001 0101 + 0110 1000
(e) Which of the following logic is fastest
 - I. TTL
 - II. ECL
 - III. CMOS
 - IV. LSI
- (f) What are *universal Gate*?
- (g) Why self-bias is more desirable than fixed bias for transistor biasing?
- (h) Discuss the advantages of SSB system in radio telephony.
- (i) What is Brakhausen criteria for sustained oscillation ?
- (j) Describe and draw the **input** and **out put** characteristic of p-n-p transistor in Common- Emitter configuration.

PART – B

Marks:5X14=70

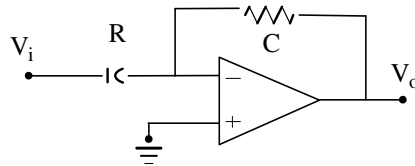
(Answer any 5 of the following)

2. (a) Implement a *full Adder* with 4:1 multiplexer [7]
(b) Briefly discuss the construction and working of **4-bit shift register** [7]
3. (a) The Si transistor of Fig has $\beta=50$ (neglect leakage current). $V_{CC}=18V$, $V_{EE} = 4V$, $R_E= 200 \Omega$, $R_C= 4 K\Omega$ a) Find R_B so that $I_{CQ}=2mA$ and also determine V_{CEQ} for same V_B [7]



(b) Explain with suitable circuit diagram *Bi-stable Multivibrator*. [7]

4. (a) Find the output voltage V_o of the circuit shown below. [7]



(b) Explain with suitable circuit diagram operation of *Instrumentation Amplifier* [7]

5. (a) Draw and explain frequency demodulation circuit. [7]

(b) The rms value of a carrier voltage after amplitude modulation to a depth of 50 % by another sinusoidal voltage is 59 volts. Calculate the rms value of carrier voltage when amplitude modulated to a depth of 70 %.

6. (a) What are the advantages of a negative feedback and Draw and explain class A Amplifier. [7]

(b) A two stage RC coupled amplifier has a voltage gain of 50. The output resistance of the amplifier is 21 K Ω . Amplifier is now provided 75% negative voltage feedback in series with the input. Calculate Voltage gain and output resistance with feedback. [7]

7. (a) Draw an equivalent circuit diagram of SCR and also explain triggering method of SCR. [7]

(b) Explain briefly operation of power meter. [7]

8. (a) With a Suitable circuit diagram explain *TTL NAND gate* [7]

(b) Write an assembly level program for 8085 microprocessor to add two number . [7]
